FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C00 • MM74C02 • MM74C04 Quad 2-Input NAND Gate • Quad 2-Input NOR Gate • Hex Inverter

General Description

The MM74C00, MM74C02, and MM74C04 logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 74 devices minimizes design time for those designers already familiar with the standard 74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power consumption: 10 nW/package (typ.)
- Low power: TTL compatibility:
  Fan out of 2 driving 74L

Ordering Code:

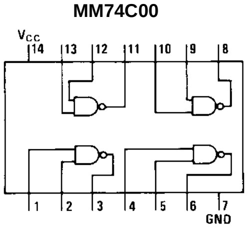
Order Number	Package Number	Package Description
MM74C00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
MM74C00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM74C02N	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
MM74C04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
MM74C04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

Connection Diagrams

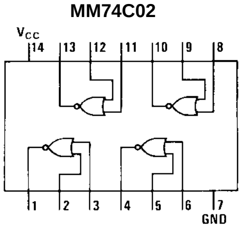
Pin Assignments for DIP and SOIC

MM74C00



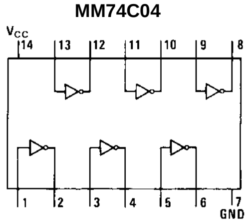
Top View

MM74C02



Top View

MM74C04



Top View

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Operating V_{CC} Range	3.0V to 15V
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 µA			0.5	V
		V_{CC} = 10V, I_O = 10 µA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	µA
LOW POWER TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	74C, V_{CC} = 4.75V, I_O = −10 µA	4.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	74C, V_{CC} = 4.75V, I_O = 10 µA			0.4	V
CMOS TO LOW POWER						
$V_{IN(1)}$	Logical "1" Input Voltage	74C, V_{CC} = 4.75V	4.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	74C, V_{CC} = 4.75V			1.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	74C, V_{CC} = 4.75V, I_O = −360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	74C, V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (see Family Characteristics Data Sheet) T_A = 25°C (short circuit current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics (Note 2)

T_A = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM74C00, MM74C02, MM74C04						
t_{pd0}, t_{pd1}	Propagation Delay Time to	V_{CC} = 5.0V		50	90	ns
	Logical "1" or "0"	V_{CC} = 10V		30	60	ns
C_{IN}	Input Capacitance	(Note 3)		6.0		pF
C_{PD}	Power Dissipation Capacitance	Per Gate or Inverter (Note 4)		12		pF

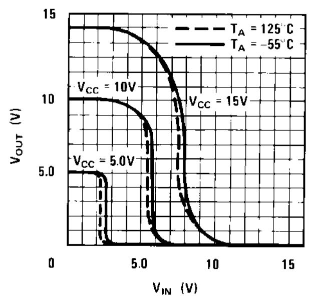
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

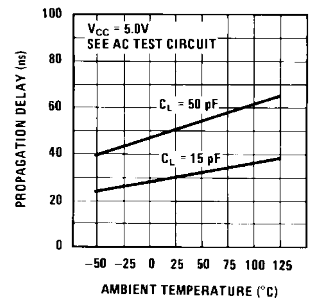
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

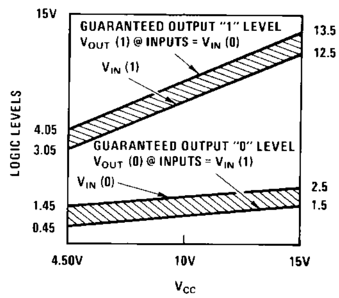
Gate Transfer Characteristics



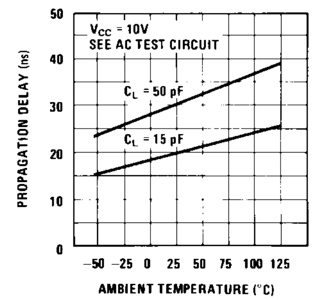
Propagation Delay vs Ambient Temperature MM74C00, MM74C02, MM74C04



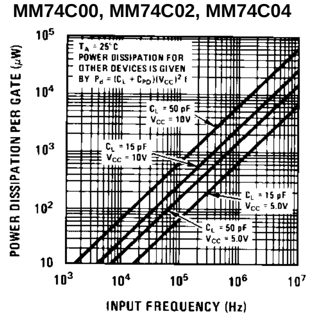
Guaranteed Noise Margin Over Temperature vs V_{CC}



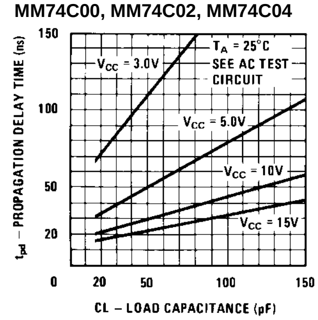
Propagation Delay vs Ambient Temperature MM74C00, MM74C02, MM74C04



Power Dissipation vs Frequency MM74C00, MM74C02, MM74C04

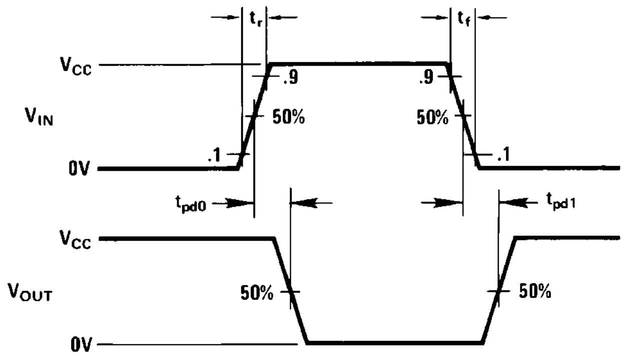


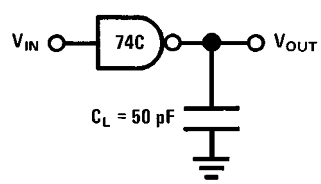
Propagation Delay Time vs Load Capacitance MM74C00, MM74C02, MM74C04



Switching Time Waveforms and AC Test Circuit

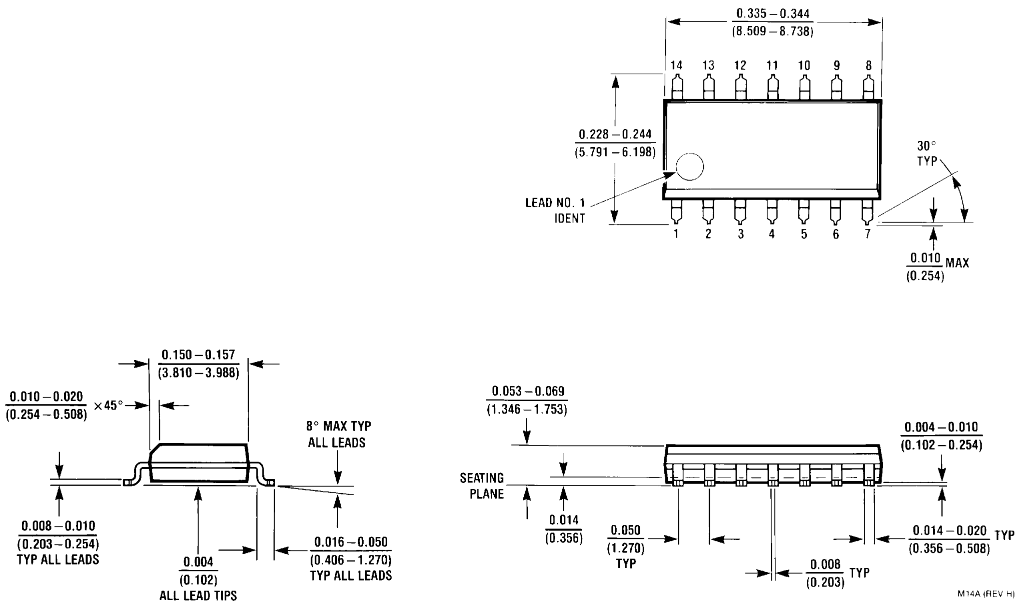
CMOS to CMOS





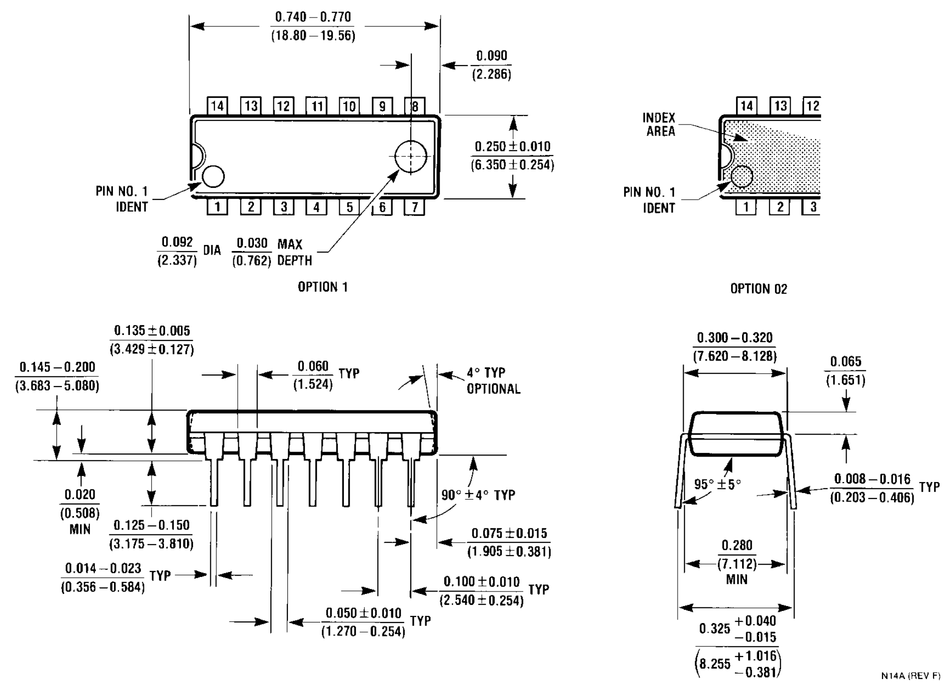
Delays measured with input t_r, $t_f \leq 20$ ns.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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